In the Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1-34. (Cancelled)

35. (New) A semiconductor device, comprising:

a field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a bonding pad connected to the gate electrode, the source electrode or the drain electrode; and

a protecting element for the transistor connected between the bonding pad and a terminal of one of the electrodes that is not connected to the bonding pad, the protecting element comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region disposed between the first and second high concentration impurity regions and being configured to permit current flow between the first and second high concentration impurity regions upon application between the bonding pad and the terminal of an electrostatic energy that is larger than a predetermined amount,

wherein at least part of the first high concentration impurity region is disposed under the bonding pad.

36. (New) The semiconductor device of claim 35, wherein the first high concentration impurity region is disposed along at least one side of the bonding pad.

37. (New) The semiconductor device of claim 35, further comprising a peripheral high concentration impurity region disposed at a peripheral area of the bonding pad, wherein the first high concentration impurity region is part of the peripheral high concentration impurity region.

38. (New) The semiconductor device of claim 35, wherein the protecting element is placed in a path extending from the terminal to an operation region of the field effect transistor.

39. (New) The semiconductor device of claim 35, further comprising:

an additional bonding pad provided as the terminal; and

a resistor connected to the additional bonding pad and comprising a resistor high concentration impurity region,

wherein the second high concentration impurity region is at least part of the resistor high concentration impurity region.

40. (New) The semiconductor device of claim 35, further comprising:

an additional bonding pad provided as the terminal; and

a metal wiring connected to the additional bonding pad,

wherein at least part of the second high concentration impurity region is disposed under the metal wiring or placed in close proximity to the metal wiring to permit the current flow upon the application of the electrostatic energy.

41. (New) The semiconductor device of claim 35, further comprising a metal electrode, wherein at least part of the second high concentration impurity region is disposed under the metal electrode or in close proximity to the metal electrode to permit the current flow upon the application of the electrostatic energy.

42. (New) The semiconductor device of claim 41, wherein the metal electrode forms a Schottky junction with a surface of a substrate, and a distance between the metal electrode and the second high concentration impurity region is less than 5 μm.

43. (New) The semiconductor device of claim 35, further comprising an additional protecting element for the transistor connected between the bonding pad and another terminal of the electrodes that is not connected to the bonding pad, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the bonding pad and the another terminal of an electrostatic energy that is larger than a predetermined amount, wherein the

protecting element is disposed along a side of the bonding pad and the additional protecting element is disposed along another side of the bonding pad.

44. (New) The semiconductor device of claim 35, further comprising:

an additional field effect transistor comprising a gate electrode, a source electrode and a drain electrode; and

an additional protecting element connected between the bonding pad and a terminal of one of the electrodes of the additional field effect transistor, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application of an electrostatic energy that is larger than a predetermined amount between the bonding pad and the terminal of the additional filed effect transistor,

wherein the protecting element is disposed along a side of the bonding pad and the additional protecting element is disposed along another side of the bonding pad.

45. (New) The semiconductor device of claim 35, further comprising:

an additional bonding pad provided as another terminal of the electrodes; and

an additional protecting element for the transistor connected between the terminal and the additional bonding pad, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the terminal and the additional bonding pad of an electrostatic energy that is larger than a predetermined amount,

wherein at least part of the first additional high concentration impurity region is disposed under the additional bonding pad or in close proximity to the additional bonding pad to permit the current flow upon the application of the electrostatic energy.

46. (New) The semiconductor device of claim 45, wherein the protecting element and the additional protecting element are placed in a path extending from the terminal to an operation region of the field effect transistor.

47. (New) The semiconductor device of claim 35, wherein an electrostatic breakdown voltage of the semiconductor device is higher at least by 20 volts than an electrostatic breakdown voltage of the semiconductor device without the protecting element.

48. (New) The semiconductor device of claim 35, wherein an electrostatic breakdown voltage of the semiconductor device is 200 volts or higher.

49. (New) The semiconductor device of claim 35, wherein the first and second high concentration impurity regions of the protecting element are separated by 10 μm or less.

50. (New) The semiconductor device of claim 35, wherein the first and second high concentration impurity regions are impurity regions of the same conduction type.

51. (New) The semiconductor device of claim 35, wherein the first and second high concentration impurity regions have an impurity concentration that is approximately equal to an impurity concentration of a source region under the source electrode or an impurity concentration of a drain region under the drain electrode.

52. (New) The semiconductor device of claim 35, wherein the insulating region is an impurity implanted region formed in a substrate.

53. (New) The semiconductor device of claim 35, wherein the insulating region is part of a semi-insulating substrate.

54. (New) The semiconductor device of claim 35, wherein the transistor is a MESFET, a junction type FET, or an HEMT.

55. (New) A semiconductor device, comprising:

a field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a bonding pad connected to the gate electrode, the source electrode or the drain electrode; and

a protecting element for the transistor connected between the bonding pad and a terminal of one of the electrodes that is not connected to the bonding pad, the protecting element comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region disposed between the first and second high concentration impurity regions and being configured to permit current flow between the first and second high concentration impurity regions upon application between the bonding pad and the terminal of an electrostatic energy that is larger than a predetermined amount,

wherein the first high concentration impurity region is connected to the bonding pad through a Schottky junction so as to permit the current flow upon the application of the electrostatic energy.

56. (New) The semiconductor device of claim 55, wherein the first high concentration impurity region is disposed along at least one side of the bonding pad.

57. (New) The semiconductor device of claim 55, further comprising a peripheral high concentration impurity region disposed at a peripheral area of the bonding pad, wherein the first high concentration impurity region is part of the peripheral high concentration impurity region.

58. (New) The semiconductor device of claim 55, wherein the protecting element is placed in a path extending from the terminal to an operation region of the field effect transistor.

59. (New) The semiconductor device of claim 55, further comprising:

an additional bonding pad provided as the terminal; and

a resistor connected to the additional bonding pad and comprising a resistor high concentration impurity region,

wherein the second high concentration impurity region is at least part of the resistor high concentration impurity region.

60. (New) The semiconductor device of claim 55, further comprising:

an additional bonding pad provided as the terminal; and

a metal wiring connected to the additional bonding pad,

wherein at least part of the second high concentration impurity region is disposed under the metal wiring or in close proximity to the metal wiring to permit the current flow upon the application of the electrostatic energy.

61. (New) The semiconductor device of claim 55, further comprising a metal electrode, wherein at least part of the second high concentration impurity region is disposed under the metal electrode or in close proximity to the metal electrode to permit the current flow upon the application of the electrostatic energy.

62. (New) The semiconductor device of claim 61, wherein the metal electrode forms a Schottky junction with a surface of a substrate, and a distance between the metal electrode and the second high concentration impurity region is less than 5 μm.

63. (New) The semiconductor device of claim 55, further comprising an additional protecting element for the transistor connected between the bonding pad and another terminal of the electrodes that is not connected to the bonding pad, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the bonding pad and the another terminal of an electrostatic energy that is larger than a predetermined amount, wherein the protecting element is disposed along a side of the bonding pad and the additional protecting element is disposed along another side of the bonding pad.

64. (New) The semiconductor device of claim 55, further comprising:

an additional field effect transistor comprising a gate electrode, a source electrode and a drain electrode; and

an additional protecting element connected between the bonding pad and a terminal of one of the electrodes of the additional field effect transistor, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application of an electrostatic energy that is larger than a predetermined amount between the bonding pad and the terminal of the additional filed effect transistor,

wherein the protecting element is disposed along a side of the bonding pad and the additional protecting element is disposed along another side of the bonding pad.

65. (New) The semiconductor device of claim 55, further comprising:

an additional bonding pad provided as another terminal of the electrodes; and

an additional protecting element for the transistor connected between the terminal and the additional bonding pad, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the terminal and the additional bonding pad of an electrostatic energy that is larger than a predetermined amount,

wherein at least part of the first additional high concentration impurity region is disposed under the additional bonding pad or in close proximity to the additional bonding pad to permit the current flow upon the application of the electrostatic energy.

66. (New) The semiconductor device of claim 65, wherein the protecting element and the additional protecting element are placed in a path extending from the terminal to an operation region of the field effect transistor.

67. (New) A semiconductor device, comprising:

a field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a bonding pad connected to the gate electrode, the source electrode or the drain electrode;

a resistor connected to a terminal of one of the electrodes that is not connected to the bonding pad and comprising a resistor high concentration impurity region; and

a protecting element for the transistor for the transistor connected between the bonding pad and the terminal, the protecting element comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region disposed between the first and second high concentration impurity regions and being configured to permit current flow between the first and second high concentration impurity regions upon application between the bonding pad and the terminal of an electrostatic energy that is larger than a predetermined amount,

wherein the first high concentration impurity region is at least part of the resistor high concentration impurity region.

68. (New) The semiconductor device of claim 67, wherein the second high concentration impurity region is disposed along at least one side of the bonding pad.

69. (New) The semiconductor device of claim 67, wherein the protecting element is placed in a path extending from the terminal to an operation region of the field effect transistor.

70. (New) The semiconductor device of claim 67, further comprising:

an additional bonding pad provided as another terminal of the electrodes; and

an additional protecting element for the transistor connected between the terminal and the additional bonding pad, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application

between the terminal and the additional bonding pad of an electrostatic energy that is larger than a predetermined amount,

wherein the first additional high concentration impurity region is at least part of the resistor high concentration impurity region and the second additional high concentration impurity region is disposed along at least one side of the additional bonding pad.

71. (New) The semiconductor device of claim 70, wherein the protecting element and the additional protecting element are placed in a path extending from the terminal to an operation region of the field effect transistor.

72. (New) The semiconductor device of claim 67, further comprising a metal electrode, wherein at least part of the second high concentration impurity region is disposed under the metal electrode or in close proximity to the metal electrode to permit the current flow upon the application of the electrostatic energy.

73. (New) The semiconductor device of claim 72, wherein the metal electrode forms a Schottky junction with a surface of a substrate, and a distance between the metal electrode and the second high concentration impurity region is less than 5 μm.

74. (New) A semiconductor device, comprising:

a field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a bonding pad;

a metal wiring connecting the bonding pad to the gate electrode, the source electrode or the drain electrode; and

a protecting element for the transistor connected between the bonding pad and a terminal of one of the electrodes that is not connected to the bonding pad, the protecting element comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region disposed between the first and second high concentration impurity regions and being configured to permit current flow between the first and second high

concentration impurity regions upon application between the bonding pad and the terminal of an electrostatic energy that is larger than a predetermined amount,

wherein at least part of the first high concentration impurity region is disposed under the metal wiring.

75. (New) The semiconductor device of claim 74, wherein the protecting element is placed in a path extending from the bonding pad to an operation region of the field effect transistor.

76. (New) The semiconductor device of claim 74, further comprising:

an additional bonding pad provided as the terminal; and

a resistor connected to the additional bonding pad and comprising a resistor high concentration impurity region,

wherein the second high concentration impurity region is at least part of the resistor high concentration impurity region.

77. (New) The semiconductor device of claim 74, further comprising a metal electrode, wherein at least part of the second high concentration impurity region is disposed under the metal electrode or in close proximity to the metal electrode to permit the current flow upon the application of the electrostatic energy.

78. (New) The semiconductor device of claim 77, wherein the metal electrode forms a Schottky junction with a surface of a substrate, and a distance between the metal electrode and the second high concentration impurity region is less than 5 μm.

79. (New) A semiconductor device, comprising:

a field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a bonding pad;

a metal wiring connecting the bonding pad to the gate electrode, the source electrode or the drain electrode; and

a protecting element for the transistor connected between the bonding pad and a terminal of one of the electrodes that is not connected to the bonding pad, the protecting element comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region disposed between the first and second high concentration impurity regions and being configured to permit current flow between the first and second high concentration impurity regions upon application between the bonding pad and the terminal of an electrostatic energy that is larger than a predetermined amount,

wherein the first high concentration impurity region is connected to the metal wiring through a Schottky junction so as to permit the current flow upon the application of the electrostatic energy.

80. (New) The semiconductor device of claim 79, wherein the protecting element is placed in a path extending from the bonding pad to an operation region of the field effect transistor.

81. (New) The semiconductor device of claim 79, further comprising:

an additional bonding pad provided as the terminal; and

a resistor connected to the additional bonding pad and comprising a resistor high concentration impurity region,

wherein the second high concentration impurity region is at least part of the resistor high concentration impurity region.

82. (New) The semiconductor device of claim 79, further comprising a metal electrode, wherein at least part of the second high concentration impurity region is disposed under the metal electrode or in close proximity to the metal electrode to permit the current flow upon the application of the electrostatic energy.

83. (New) The semiconductor device of claim 82, wherein the metal electrode forms a Schottky junction with a surface of a substrate, and a distance between the metal electrode and the second high concentration impurity region is less than 5 μm.

84. (New) A semiconductor switching device, comprising:

a first field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a second field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a common input terminal connected to the source or drain electrode of the first transistor and to the source or drain electrode of the second transistor;

a first control terminal connected to the gate electrode of the first or second transistor;

a second control terminal connected to the gate electrode of the first or second transistor that is not connected to the first control terminal;

a first output terminal connected to the source or drain electrode of the first transistor that is not connected to the common input terminal;

a second output terminal connected to the source or drain electrode of the second transistor that is not connected to the common input terminal; and

a protecting element connected between the common input terminal and the first control terminal, the protecting element comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region disposed between the first and second high concentration impurity regions and being configured to permit current flow between the first and second high concentration impurity regions upon application between the common input terminal and the first control terminal of an electrostatic energy that is larger than a predetermined amount.

85. (New) The semiconductor switching device of claim 84, further comprising an additional protecting element connected between the first control terminal and the first output terminal or between the second control terminal and the second output terminal, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second

additional high concentration impurity regions upon application between the corresponding terminals of an electrostatic energy that is larger than a predetermined amount.

86. (New) The semiconductor switching device of claim 85, further comprising a resistor comprising a resistor high concentration impurity region, wherein the first impurity region and the first additional impurity region is are least part of the resistor high concentration impurity region.

87. (New) The semiconductor switching device of claim 84, further comprising an additional protecting element connected between the common input terminal and the second control terminal, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the corresponding terminals of an electrostatic energy that is larger than a predetermined amount, wherein the protecting element is disposed along a side of the common input terminal and the additional protecting element is disposed along another side of the common input terminal.

88. (New) The semiconductor switching device of claim 84, wherein the common input terminal comprises a bonding pad, and at least part of the first high concentration impurity region is disposed under the bonding pad.

89. (New) The semiconductor switching device of claim 88, wherein the first high concentration impurity region is disposed along at least one side of the bonding pad.

90 (New) The semiconductor switching device of claim 84, wherein the common input terminal comprises a bonding pad, and at least part of the first high concentration impurity region is placed in close proximity to the bonding pad to permit the current flow upon the application of the electrostatic energy.

91. (New) The semiconductor switching device of claim 90, wherein the first high concentration impurity region is disposed along at least one side of the bonding pad.

92. (New) The semiconductor switching device of claim 88, further comprising a peripheral high concentration impurity region disposed at a peripheral area of the bonding pad, wherein the first high concentration impurity region is part of the peripheral high concentration impurity region.

93. (New) The semiconductor switching device of claim 90, further comprising a peripheral high concentration impurity region disposed at a peripheral area of the bonding pad, wherein the first high concentration impurity region is part of the peripheral high concentration impurity region.

94. (New) The semiconductor switching device of claim 84, further comprising a resistor comprising a resistor high concentration impurity region, wherein the first control terminal comprises a bonding pad connected to the resistor, and the first high concentration impurity region is at least part of the resistor high concentration impurity region.

95. (New) The semiconductor switching device of claim 88, further comprising a resistor comprising a resistor high concentration impurity region, wherein the first control terminal comprises a bonding pad connected to the resistor, and the second high concentration impurity region is at least part of the resistor high concentration impurity region.

96. (New) The semiconductor switching device of claim 90, further comprising a resistor comprising a resistor high concentration impurity region, wherein the first control terminal comprises a bonding pad connected to the resistor, and the second high concentration impurity region is at least part of the resistor high concentration impurity region.